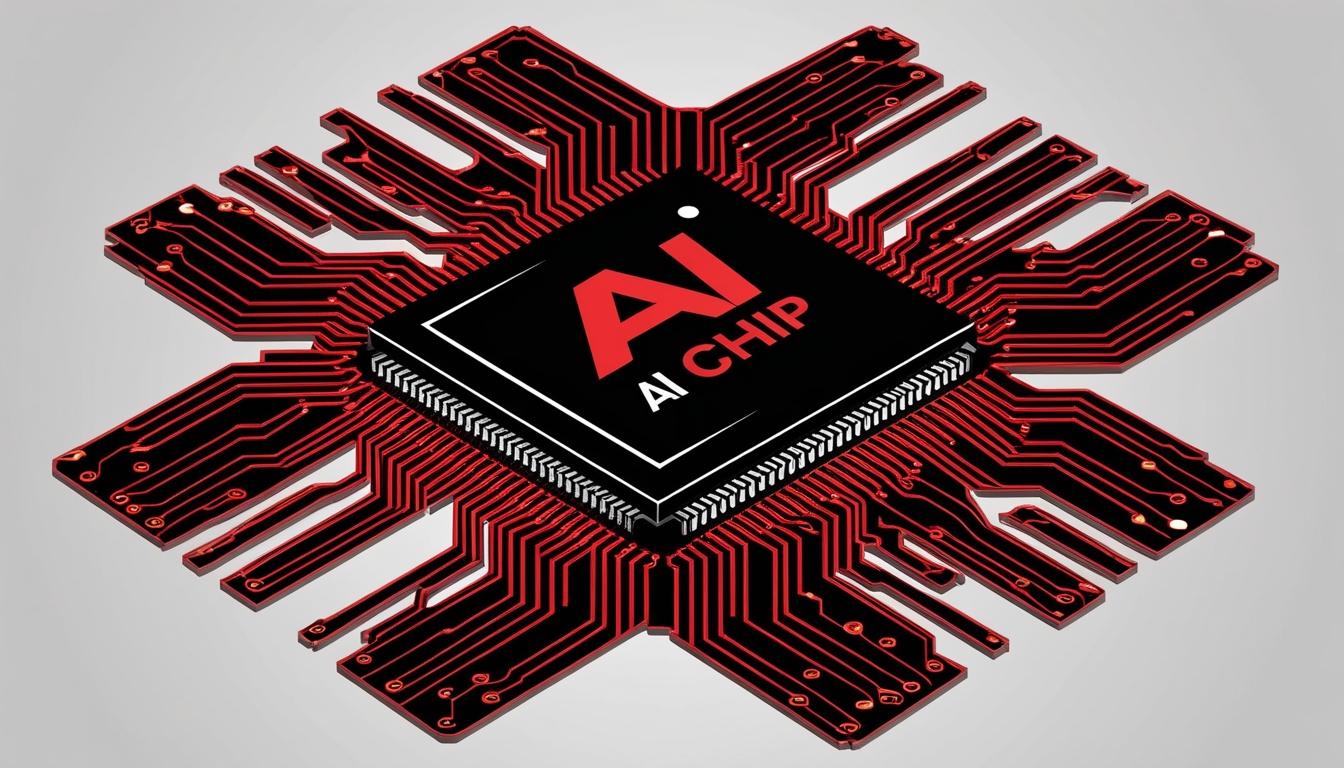
# DesignCon to focus on AI and machine learning technologies



Artificial intelligence (AI) and machine learning technologies have become critical focal points in industry discussions, particularly at technical conferences. One such event, Informa's DesignCon Show, will be held from January 28th to 30th at the Santa Clara Convention Center in Santa Clara, California. The event aims to address various technical aspects concerning AI implementation, covering a range of topics from signal integrity to memory solutions.

Among the presentations scheduled for the show is a panel discussion titled “Powering the AI Semiconductor Stack: Power Strategies for High-Performance AI Computing,” which will take place on January 28th from 4:45 to 6:00 pm in Ballroom C. This panel aims to examine the escalating power demands of contemporary AI chips and potential strategies for managing these requirements. Participants are expected to include integrated circuit (IC) customers and power infrastructure suppliers, fostering a dialogue about the future of power needs in AI.

On the following day, January 29th, Dr. Steven Woo from Rambus will present “Technology Advancements for AI in the Data Center” from 8:00 to 8:45 am in Great America Ballroom 1. This session will focus on the essential memory, interface, and security technologies required for optimising advanced AI computing capabilities within data centres.

Following Dr. Woo’s presentation, another session titled “Accelerating AI Workloads with Composable Memory and Hardware Acceleration” will take place from 9:00 to 9:45 am in the same location. In this presentation, speakers will explore innovative methods for integrating composable memory solutions with AI while leveraging Rambus' CXL intellectual property (IP) and hardware-accelerated compression IP. The discussion will highlight potential performance enhancements for applications like Meta Cachelib, a prevalent hyperscale caching solution utilised in AI services.

Later in the day, from 2:00 to 2:45 pm, the panel “How Will AI Applications Affect High Speed Link Design?” will examine the implications of AI on high-speed signal integrity. This session will address the effects of AI applications on power integrity and signal maintenance across various domains, including IC design and the power grid.

At 3:00 pm on January 29th, a critical session titled “GDDR Memory for High-Performance AI Inference” will conclude the day's discussions. This presentation will focus on advancements in GDDR7 memory technology, showcasing collaboration between Rambus and Cadence in developing integrated memory subsystems. The session will also delve into the signal integrity challenges encountered with the implementation of GDDR6 and GDDR7 at elevated data transfer rates.

The conference will wrap up on January 30th with a panel titled “Power Delivery Strategies for AI & Data Center ASICs: Horizontal vs. Vertical,” scheduled for 4:00 pm. This discussion will dissect two contrasting paradigms in power delivery—horizontal and vertical approaches. The emphasis will be on the vertical methodology, where voltage regulator modules (VRMs) are situated directly underneath ASICs and processors, a design that proponents argue reduces power plane losses by consolidating necessary capacitors within the module package.

DesignCon stands as an important platform for engineers and experts to exchange ideas and information regarding the evolving landscape of AI technologies and their impact on business practices. As AI continues to advance, discussions like these at DesignCon may yield insights necessary for navigating the complex challenges ahead in the technology sector.

Source: [Noah Wire Services](https://www.noahwire.com)

## Bibliography

1. <https://www.kgs-ind.com/exhibition/designcon2025/> - Corroborates the dates and location of DesignCon 2025 at the Santa Clara Convention Center.
2. <https://www.designcon.com/en/faqs.html> - Provides details on the event schedule, health and safety measures, and other logistical information for DesignCon 2025.
3. <https://www.kgs-ind.com/exhibition/designcon2025/> - Mentions the expo days and hours, which align with the conference schedule.
4. <https://www.chetanpatil.in/the-ai-semiconductor-stack/> - Discusses the AI semiconductor stack, including power demands, memory management, and data logic, which are relevant to the panel discussions at DesignCon.
5. <https://www.freedomlab.com/posts/the-ai-chips-race-part-ii> - Explores the role of Big Tech in AI chips and the importance of AI stacks, which is relevant to the discussions on AI computing capabilities at DesignCon.
6. <https://www.kgs-ind.com/exhibition/designcon2025/> - Confirms the event's focus on education, exhibits, and networking, particularly in the context of high-speed communications and system design.
7. <https://www.designcon.com/en/faqs.html> - Details the conference schedule, including the specific dates and times for various sessions, which matches the described sessions at DesignCon.
8. <https://www.chetanpatil.in/the-ai-semiconductor-stack/> - Addresses the escalating power demands of AI chips and strategies for managing these requirements, a topic covered in the panel discussion on January 28th.
9. <https://www.freedomlab.com/posts/the-ai-chips-race-part-ii> - Highlights the importance of memory, interface, and security technologies for AI computing, aligning with Dr. Steven Woo's presentation on January 29th.
10. <https://www.kgs-ind.com/exhibition/designcon2025/> - Emphasizes the event's role as a platform for engineers and experts to discuss AI technologies and their impact, reflecting the overall purpose of DesignCon.
11. <https://www.designcon.com/en/faqs.html> - Mentions the health and safety measures and logistical details, ensuring the event is conducted in a safe and controlled environment.
12. <https://www.designnews.com/artificial-intelligence/design-engineering-and-ai-join-forces-at-designcon> - Please view link - unable to able to access data